AMENDMENTS TO THE SPECIFICATION

The following is a marked up version of each replacement paragraph and/or section of the specification in which underlines indicate insertions and strikethrough indicates deletions.

On page 5, please replace the last two paragraphs, containing lines 22-38, with the following paragraphs:

Each of the sixteen data registers is connected to a respective one of sixteen pipelines. FIG. 3 shows only the pipelines 40, 41, 42, and 43, which are connected to respective data registers 30, 31, 32, and 33. After two data registers 30 and 32 received data in response to column cycle signal COLCYC<0>, the two data [[resisters]] resistors 30 and 32 transmit the data bits to pipelines 40 and 42. The pipelines 40 and 42 sequentially transmit data bits from each stage to the succeeding stage in a transmission operation in response to a clock signal (not shown). The pipelines 40 and 42 serially transmit the output data DATA to channel bus lines C_DQA0 and C_DQB0 through the output driers 50 and 52, respectively. Accordingly, one RDRAM 11 outputs two data bits, one bit applied to each of the channel bus lines C_DQA0 and ~~C_DQB0.~~

The remaining RDRAMs 12 through 14 of FIG. 1 perform similar output operations, for example, through output drivers 51 and 53 to drive data signals on the remaining channel bus lines. Two DQ blocks different from those of the RDRAM 11 are selected in each RDRAM 12 through 14 so that each RDRAM transmits data to a different pair of channel bus lines. Accordingly, the eight RDRAMs transmit to all sixteen bus lines C_DQA0 through C_DQA7 and C_DQB0 through C_DQB7. Therefore, the operation complies with the x16 data input/output regulation. Such operation is referred to herein as an interleave device mode.